In the Specification:

Please replace the paragraph beginning at page 2, Line 9 with the following rewritten paragraph:

--However, in recent years, techniques for pirating of integrated circuits have considerably improved and nowadays involve sophisticated analysis methods based on the observation of the current used by the elements in the integrated circuit during the execution of confidential operations. Presently, there are two types of methods for analyzing the current used, namely the SPA analysis methods (Single Power Analysis) and the DPA analysis methods (Differential Power Analysis). DPA analysis methods, which are more efficient than the former methods, allow a secret key to be revealed via a single observation of changes in the current used by the encryption circuit, without having to read the data flowing in the integrated circuit internal bus and to identify the memories that are read. Such a method relies upon a correlation of samples of the current used with a mathematical model of the encryption circuit and assumptions about the secret key's value. The correlation allows the dc-component in the used current to be suppressed and consumption peaks to be revealed which show the operation performed by the encryption circuit and confidential data values. With such a method, only about 1000 samples need to be recorded for a ~~DES~~ Data Encrytpion Standard (DES) secret key to be obtained.--

Please replace the paragraph beginning at page 5, Line 27 with the following rewritten paragraph:

--According to yet another feature of this invention, the integrated circuit comprises a Metal-Oxide-

Semiconductor (MOS) ~~MOS~~ transistor having very small leakage currents, which is associated with the capacitor, so that it is only discharged by the leakage currents when the integrated circuit is powered-off. Preferably, it also comprises a test circuit, which is controlled by a test control command, for reducing the timing period. (It is noted that the "metal oxide" in MOS comes from the first devices that used a metal gate over oxide (silicon dioxide); subsequently, poly-crystalline silicon has been used for the gate, and the term MOS now at least includes both.)--

Please replace the paragraph beginning at page 7, Line 11 with the following rewritten paragraph:

--Fig. 1 diagrammatically shows the construction of an integrated circuit 1 for smart cards. This integrated circuit 1 comprises a central processor unit 2, for example a microprocessor or microcontroller, a communication unit 7 enabling communications with an external terminal 10, an encryption circuit 6 and memories 4, namely a read only memory in which is stored the operating system of CPU 2, a Random Access Memory (RAM) ~~RAM~~ memory for storing temporary data, and a programmable and erasable memory, for example an Electrically Erasable Programmable Read-Only Memory (EEPROM), for storing one or more application programs. CPU 2, memories 4, encryption circuits 6, and communication unit 7 are interconnected through a common data bus 3.--

Please replace the paragraph beginning at page 8, Line 1 with the following rewritten paragraph:

--In Fig. 2, this circuit 5 comprises a timer circuit, which includes an n-channel MOS (nMOS) ~~nMOS~~ transistor M1 advantageously designed to have a very small drain-source leakage current, i.e. of minimum drain perimeter and surface. This transistor has its drain connected to the ground through another nMOS transistor 27, the gate of which is coupled to a discharge control input Dchrg. The drain of transistor M1 is also coupled through a diode D1 reverse-connected to the drain of a p-channel MOS (pMOS) ~~pMOS~~ transistor 24 having its source coupled to the voltage source V_{dd}. The gate of transistor 24 is connected to the output of an inverter 25 whose input is connected to the output of an OR gate 23. This OR gate 23 has a first input connected to the charge control input Chrg of circuit 5, and a second input connected to output Q of circuit 5.--

Please replace the paragraph beginning at page 8, Line 1 with the following rewritten paragraph:

--Additionally, the source of transistor M1 is connected, on the one hand, to the ground through a capacitor C, and on the other hand, to output Q of circuit 5 through two series-connected inverter stages for transforming the voltage across capacitor C into a logic signal. Conventionally, each inverter stage comprises a pMOS transistor 28 ~~20~~, 30, and an nMOS transistor 29, 31, which are series-connected between voltage source V_{dd} and the ground. Transistors 21 to 31 are constructed so that a very small voltage across the capacitor provides a logic level 1 at output Q.--